WEST

Help | Logout | Interrupt

Main Menu | Search Form | Posting Counts | Show S Numbers | Edit S Numbers | Preferences | Cases

Search Results -

Terms	Documents
hub near2 graphics near3 (module or engine or section or unit or block or accelerator or subsystem or sub-system or logic or circuit$3 or interface)	4

Database: US Patents Full-Text Database
US Pre-Grant Publication Full-Text Database
JPO Abstracts Database
EPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L2

Refine Search

Recall Text | Clear

Search History

DATE: Wednesday, June 04, 2003 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
	DB=USPT; PLUR=YES; OP=ADJ		
L2	hub near2 graphics near3 (module or engine or section or unit or block or accelerator or subsystem or sub-system or logic or circuit$3 or interface)	4	L2
L1	hub near2 graphics adj3 (module or engine or section or unit or block or accelerator or subsystem or sub-system or logic or circuit$3 or interface)	1	L1

END OF SEARCH HISTORY

WEST

Generate Collection | Print

Search Results - Record(s) 1 through 4 of 4 returned.

☐ 1. Document ID: US 6574738 B2

L2: Entry 1 of 4 File: USPT Jun 3, 2003

DOCUMENT-IDENTIFIER: US 6574738 B2
TITLE: Method and apparatus to control processor power and performance for single phase lock loop (PLL) processor systems

Abstract Text (1):
An integrated circuit contains a central processing unit ("CPU"), a graphic control hub ("GCH"), a memory control hub ("MCH"), and a phase lock loop ("PLL"). The GCH, MCH, and PLL are coupled to the CPU. The MCH controls memory transactions. The PLL is configured to allow the CPU to operate at more than one power consumption states.

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw Desc | Image

☐ 2. Document ID: US 6442697 B1

L2: Entry 2 of 4 File: USPT Aug 27, 2002

DOCUMENT-IDENTIFIER: US 6442697 B1
** See image for Certificate of Correction **
TITLE: Method and apparatus to control processor power and performance for single phase lock loop (PLL) processor systems

Abstract Text (1):
An integrated circuit contains a central processing unit ("CPU"), a graphic control hub ("GCH"), a memory control hub ("MCH"), and a phase lock loop ("PLL"). The GCH, MCH, and PLL are coupled to the CPU. The MCH controls memory transactions. The PLL is configured to allow the CPU to operate at more than one power consumption states.

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw Desc | Image

☐ 3. Document ID: US 6374317 B1

L2: Entry 3 of 4 File: USPT Apr 16, 2002

DOCUMENT-IDENTIFIER: US 6374317 B1
** See image for Certificate of Correction **
TITLE: Method and apparatus for initializing a computer interface

CLAIMS:

5. The computer system of claim 3 wherein the first hub agent is a network interface card and the second hub agent is a graphics accelerator.

☐ 4. Document ID: US 6133919 A

L2: Entry 4 of 4 File: USPT Oct 17, 2000

DOCUMENT-IDENTIFIER: US 6133919 A
TITLE: Method and apparatus for using a graphical user interface (GUI) as the interface to a distributed platform switch

Detailed Description Text (16):
Each switch element can include at least one redundant unit. The GUI can indicate the operational status of all redundant units for each switch element. For example, in the case where hub 110 has two redundant units, the graphic presentation of hub 110 in the GUI can comprise two halves each with its own color to indicate the status of both hub units.

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Drawi Desc | Image

Generate Collection Print

Terms	Documents
hub near2 graphics near3 (module or engine or section or unit or block or accelerator or subsystem or sub-system or logic or circuit$3 or interface)	4

Display Format: KWIC Change Format

Previous Page Next Page